REMARKS

It is noted that claims 70-73 are found allowable.

The Examiner has rejected claims 63-69 under 35 U.S.C. §112, first paragraph for lack of support from the specification. Specifically, the Examiner contends that independent claim 63 lacks support in reciting "writing data into at least some of the erased first combination of sectors, followed by the designation of a second combination different from the first combination, followed by the step of erasing the second combination, and after the erasure of the second combination writing data into at least some of the second combination."

Claims 63-69 are being cancelled in this application. New claims 85-92 are being added in this application. The new claims are more compact and are believed supported in the specification. For example, in the specification

page 6, lines 18-22:

> One aspect of the present invention is the substitution of a specific type of semiconductor memory system for the disk drive but without having to sacrifice non-volatility, ease of erasing and rewriting data into the memory ...

page 8, lines 7-15:

> In system designs that store data in files or blocks the data will need to be periodically updated with revised or new information. It may also be desirable to over-write some no longer needed information. In a Flash Eeprom memory, the memory cells must first be erased before information is placed in them. That is, a write (or program) operation is always preceded by an erase operation.

These passages disclose that the EEPROM memory system is operating like, and in place of, a disk drive. The files therein are stored in blocks or sectors and will be periodically updated with revised or new information. Such an update or program operation will always be preceded by an erase operation.

Thus in new independent claim 85, the language reciting "writing data into at least some of the erased combination of

sectors" is supported in the specification by "a write (or program) operation is always preceded by an erase operation", and "periodically updated with revised or new information. It may also be desirable to over-write some no longer needed information." The repeating of the operations (a) through (c) is supported by "... periodically updated with revised or new information. It may also be desirable to over-write some no longer needed information."

The Examiner has rejected claims 74, 75, 78/74, 79/74, 79/75, 80, 81, 84/80 and 84/81 under 35 U.S.C. §102(b) as being anticipated by Mitsuishi et al.

Independent claim 74 is directed to a multiple sector erase memory device that includes a memory controller which sends signals to a logic circuit configured to address and enable a plurality of sectors for erasure. This allows efficient application of flash memory as mass storage so as to replace magnetic disk drives. The memory is partitioned into a plurality of flash sectors, the cells of the individual sectors being erasable together. The invention calls for efficient erase by selecting a combination of sectors and erasing them together.

Mitsuishi et al. discloses a memory card device having security features and teaches the opposite of the present invention, namely, how to prevent erasing and reprogramming of certain rows permanently. This is useful for security storage cards where sensitive and accounting data must be protected from being tampered with.

Three embodiments are disclosed in Mitsuishi et al. The first embodiment discloses a device that erases either a single row or the entire memory chip. The memory chip contains a "protected" row storing protective information such as serial No. and an identifying code. During the chip erase, the protective information is preserved by temporarily being stored in the column latches. At the end of the erase operation, the protective information can be rewritten into the protected row. In the second embodiment, the identity of the protected rows are permanently stored in the first row (row 11) of the memory array. There is no disclosure of permitting a user to rewrite the data in row 11 to

alter the identity of the erase inhibited rows. This is consistent with the security considerations that motivates Mitsuishi et al. in the first place (see for example col. 9, line 66 to col. 10, line 14.) In the third embodiment, a single-chip microcomputer for an IC card in which the EEPROM of the first or second embodiment is built.

Thus, Mitsuishi et al. does not disclose employing a memory controller which sends signals to a logic circuit configured to address and enable a plurality of sectors for erasure; furthermore, it actually teaches away from it.

Claims 70 to 91 are now pending. Reconsideration of the rejection is respectfully requested in view of the amendment and explanations.

Respectfully submitted,

Dated: December 23, 1996

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